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UTILITY PATENT APPLICATION TRANSMITTAL

(Only for new nonprovisional applications under 37 CFR 1.53(b))

Attorney Docket No.	004509.P005
First Inventor or Application Identifier	Richard Wissler Stallkamp
Title	A METHOD OF GENERATING TIMESTAMPS FOR ISOCHRONOUS DATA
Express Mail Label No.	EM014066455US

09/544738 U.S. PTO 04/07/00

jc712

APPLICATION ELEMENTS

See MPEP chapter 600 concerning utility patent application contents

ADDRESS TO: Assistant Commissioner for Patents, Box Patent Application, Washington, DC 20231

1. [X] Fee Transmittal Form *(e.g. PTO/SB/17)* *(Submit an original, and a duplicate for fee processing)*
2. [X] Specification — Total Pages: 22 *(preferred arrangement set forth below)*
   - Descriptive title of the Invention
   - Cross References to Related Applications
   - Statement Regarding Fed sponsored R & D
   - Reference to Microfiche Appendix
   - Background of the Invention
   - Brief Summary of the Invention
   - Brief Description of the Drawings *(if filed)*
   - Detailed Description
   - Claim(s)
   - Abstract of the Disclosure
3. [X] Drawing(s) *(35 U.S.C.113)* — Total Sheets: 4
4. Oath or Declaration — Total Pages: 3
   - a. [X] Newly executed (original copy)
   - b. [ ] Copy from a prior application (37 CFR 1.63(d)) *(for continuation/divisional with Box 16 completed)*
     - i. [ ] DELETION OF INVENTOR(S) Signed statement attached deleting inventor(s) named in the prior application, see 37 CFR 1.63(d)(2) and 1.33(b).

NOTE FOR ITEMS 1 & 13. IN ORDER TO BE ENTITLED TO PAY SMALL ENTITY FEES, A SMALL ENTITY STATEMENT IS REQUIRED (37 C.F.R. § 1.27), EXCEPT IF ONE FILED IN A PRIOR APPLICATION IS RELIED UPON (37 C.F.R. § 1.28).

5. [ ] Microfiche Computer Program *(Appendix)*
6. Nucleotide and/or Amino Acid Sequence Submission *(if applicable, all necessary)*
   - a. [ ] Computer Readable Copy
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ACCOMPANYING APPLICATION PARTS

7. [X] Assignment Papers (cover sheet & document(s))
8. [ ] 37 CFR 3.73(b) Statement *(when there is an assignee)* [ ] Power of Attorney
9. [ ] English Translation Document *(if applicable)*
10. [ ] Information Disclosure Statement (IDS)/PTO - 1449 [ ] Copies of IDS Citations
11. [ ] Preliminary Amendment
12. [X] Return Receipt Postcard (MPEP 503) *(Should be specifically itemized)*
13. [ ] *Small Entity Statement(s) [ ] Statement filed in prior application, Status still proper and desired
14. [ ] Certified Copy of Priority Document(s) *(if foreign priority is claimed)*
15. [ ] Other: . . . . . .

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[ ] Continuation [ ] Divisional [ ] Continuation-in-part (CIP) of prior application No: ____/____

Prior application Information: Examiner ____ *Group/Art Unit:* ____

For CONTINUATION or DIVISIONAL APPS only: The entire disclosure of the prior application, from which an oath or declaration is supplied under Box 4b, is considered a part of the disclosure of the accompanying continuation or divisional application and is hereby incorporated by reference. The incorporation can only be relied upon when a portion has been inadvertently omitted from the submitted application parts.

17. CORRESPONDENCE ADDRESS

[ ] *Customer Number or Bar Code Label* *(Insert Customer No. or Attach bare code label here)* or [X] *Correspondence address below*

Name	BLAKELY, SOKOLOFF, TAYLOR & ZAFMAN LLP				
Address	12400 Wilshire Boulevard, Seventh Floor				
City	Los Angeles	State	California	Zip Code	90025
Country	U.S.A.	Telephone	(310) 207-3800	Fax	(310) 820-5988

Name (Print/Type)	Thomas M. Coester, Reg. No. 39,637		
Signature	Thomas Coester	Date	4/6/00

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Docket No. 004509.P005
Express Mail No.: EM014066466US

UNITED STATES PATENT APPLICATION

FOR

A METHOD OF GENERATING TIMESTAMPS FOR ISOCHRONOUS DATA

INVENTOR:

RICHARD WISSLER STALLKAMP

PREPARED BY:

BLAKELY, SOKOLOFF, TAYLOR & ZAFMAN, LLP
12400 WILSHIRE BOULEVARD
SEVENTH FLOOR
LOS ANGELES, CA 90025-1026

(503) 684-6200

A METHOD OF GENERATING TIMESTAMPS FOR ISOCHRONOUS DATA

BACKGROUND OF THE INVENTION

1. Field of the Invention

The present invention generally relates to the field of audio and video processing. More specifically, the present invention relates to a method of generating timestamps for isochronous data.

2. Background Information

One characteristic that all isochronous transport mechanisms share is the ability to transmit data within certain fixed time constraints whereby maximum data latency and minimum bandwidth allocation is guaranteed. Isochronous transport mechanisms are useful, for example, in the transfer of multimedia data where synchronization of audio and video upon playback is important. To that end, a sound or picture transmitted from a device such as a digital video camera, across a network to a display device, for example, should be received at the display device at nearly the same rate the data was transmitted from the video camera.

Isochronous networks typically grant the highest priority access to a device known as a cycle master that maintains a common clock source for the network. Timing information is exchanged within isochronous networks through the use of timestamps within network packets. Using timestamps, the cycle master transmits to all isochronous nodes, a periodic timing request known as a "cycle start" indicating the start of each isochronous cycle. Each node with isochronous service contains a 32-bit

"cycle timer register". The low-order 12-bits of the register represent a modulo 3072 count, which increments once every 24.576 MHz clock period. The next 13 higher order bits represent a count of 8 kHz cycles, and the highest 7 bits represent a count of seconds. If a cycle start is delayed, the amount of time that the cycle start was delayed is encoded within the data packet which is broadcast to the cycle timer register of each node on the network. The cycle master copies its cycle timer register to all isochronous nodes along with the cycle start request, thereby synchronizing all nodes to be within a constant phase difference.

The IEEE Standard for a High Performance Serial Bus, IEEE Std. 1394-1995 published August 30, 1996 (1394-1995 Standard) and its progeny provide a high speed serial protocol which permits implementation of high speed data transfers of both asynchronous and isochronous data. The existing progeny includes P1394a Draft Standard for a High Performance Serial Bus (1394a Standard) and P1394b Draft Standard for a High Performance Serial Bus (1394b Standard). Generically, networks implementing 1394-1995, 1394a, 1394b or subsequent revisions and modifications thereof are referred to herein as IEEE 1394 networks. Additionally, information regarding a general isochronous packet format used in conjunction with IEEE 1394 may be found in the International Electrotechnical Commission standard 61883-1:1998-02 (hereinafter "IEC 61883").

In order to preserve data ordering on an IEEE 1394 network, each isochronous packet of audio/video data is time-stamped before it is transmitted. Each timestamp is based upon the current cycle-time of the isochronous network as determined by the cycle master. It is possible, however, that the audio/video data may have been

generated based upon an external reference signal (e.g. a house reference signal) having an operating frequency that is asynchronous to that of the cycle master. Because isochronous packets are consumed (i.e. replayed) at destination nodes according to the packet's respective isochronous timestamps independent of the frequency at which the data was originally generated, audio/video playback may be adversely affected if the reference clocks and IEEE 1394 clocks are allowed to drift from one another. Furthermore, because isochronous packets are based on a first time domain as determined by the cycle master, and audio/video data is based upon a second time domain, typically a house reference signal, it is often difficult to accurately reconstruct audio/video data after it has been transmitted over an isochronous network.

BRIEF DESCRIPTION OF THE DRAWINGS

The invention is illustrated by way of example, and not by way of limitation in the figures of the accompanying drawings in which like reference numerals refer to similar elements.

Figure 1 is a block diagram illustrating an exemplary audio/video communication network including an isochronous transport medium.

Figure 2 is a block diagram illustrating an audio/video device according to one embodiment of the present invention.

Figure 3 is a block diagram illustrating a synchronization circuit according to one embodiment of the present invention.

Figure 4 is a block diagram illustrating frequency locking logic according to one embodiment of the present invention.

DETAILED DESCRIPTION

A method of generating timestamps for isochronous data is disclosed. In the following description, for purposes of explanation, numerous specific details are set forth in order to provide a thorough understanding of the present invention. It will be apparent, however to one skilled in the art that the present invention can be practiced without these specific details. In other instances, well-known structures and devices are shown in block diagram form to avoid obscuring the present invention.

The present invention also relates to an apparatus for performing the operations described herein. This apparatus may be specially constructed for the required purposes, or it may comprise a general purpose computer selectively activated or reconfigured by a computer program stored in the computer. Such a computer program may be stored in a computer readable storage medium, such as, but is not limited to, any type of disk including floppy disks, optical disks, CD-ROMS, magneto-optical disks, read-only memories (ROMs), random access memories (RAMs), EPROMs, EEPROMs, magnetic or optical cards, or any type of media suitable for storing electronic instructions, and each coupled to a computer system bus. The algorithms and displays presented herein are not inherently related to any particular computer or other apparatus. Various general purpose machines may be used with programs in accordance with the teachings herein, or it may prove convenient to construct more specialized apparatus to perform the required method steps. The required structure for a variety of these machines will appear from the description below.

Although all or some of the operations may be performed by software executing on one or more processing devices (e.g., CPUs) on a computer system or specialized apparatus, some or all of these operations may be performed by digital logic and/or circuitry, as well as an integrated circuit (e.g., ASIC) or other semiconductor substrates. Reference in the specification to "one embodiment" or "an embodiment" means that a particular feature, structure, or characteristic described in connection with the embodiment is included in at least one embodiment of the invention. The appearances of the phrase "in one embodiment" in various places in the specification are not necessarily all referring to the same embodiment.

Figure 1 is a block diagram illustrating audio/video (A/V) devices 108 and 110 coupled to isochronous transport medium 104 as well as reference signal line 102. A/V devices 108 and 110 represent a broad range of audio and/or video components known in the art to process audio and/or video data. For example, A/V devices 108 and 110 may represent one or more audio and video recording, generation, and/or playback devices. In one embodiment, at least one of A/V devices 108 and 110 represents a digital video camera equipped to generate and record digital video images in addition to recording associated audio signals.

Isochronous transport medium (hereinafter "isochronous network") 104 represents a data distribution network configured to transmit data within certain fixed time constraints as determined by a cycle master. Master 106 represents a device equipped to function as a cycle master for isochronous network 104. As a cycle master, master 106 maintains a clock signal common to all nodes connected to isochronous network 104 including A/V devices 108 and 110. Master 106 periodically transmits

cycle start signals across isochronous network 104 to alert the variously connected devices as to when to begin data transmission. In one embodiment, network 104 is an IEEE 1394 compliant communications network and master 106 is equipped to function as a cycle master in accordance with the IEEE 1394 standard. Although master 106 may additionally possess the functionality of any number of audio and/or video devices known in the art, for the purpose of this disclosure such functionality need not be described. Likewise, although A/V devices 108 and 110 are described as merely representing nodes on an isochronous network, it will be apparent to one skilled in the art that either of A/V devices 108 and 110 may additionally be equipped to function as a cycle master in lieu of master 106.

Reference signal line 102 represents a signal line by which synchronization signals may be transmitted to one or more devices, such as A/V devices 108 and 110, such that the devices operate according to the same operating frequency. In one embodiment, reference signal line 102 represents a coaxial distribution bus configured to distribute a house reference signal (also known as "video black") to the various audio/video devices connected to signal line 102. In one embodiment, reference signal line 102 distributes a synchronization signal that is asynchronous to the isochronous clock signal distributed across isochronous network 104 by master 106.

Figure 2 is a block diagram further illustrating A/V device 108 according to one embodiment of the present invention. A/V device 108 includes processor 201 to process signals and execute stored instructions. Processor 201 may represent a complex instruction set computing (CISC) microprocessor, a reduced instruction set computing (RISC) microprocessor, a processor implementing a combination of instruction sets, or

some other processing device known in the art. Although Figure 2 illustrates a single processor 201, it will be appreciated that A/V device 108 may comprise multiple processing devices.

Processor 201 is coupled to CPU bus 210 that transmits data signals between processor 201 and other components of A/V device 108 by way of bridge/memory controller 212. Bridge/memory controller 212 is coupled to CPU bus 210, memory 213, and first I/O bus 220 to direct data signals between the respective components. Memory 213 represents a memory storage device such as dynamic random access memory (DRAM), synchronous dynamic random access memory (SDRAM), or any other volatile or non-volatile memory device known in the art. In one embodiment, memory 213 temporarily stores instructions and code represented by data signals that, when executed by processor 201, cause A/V device 108 to perform various functions described herein. As will be appreciated by those skilled in the art, A/V device 108 may additionally include a cache memory (not shown) coupled either directly or indirectly to processor 201.

First I/O bus 220 represents one or more data buses such as an IEEE 1394 backplane, a Peripheral Component Interconnect (PCI) bus, a Personal Computer Memory Card International Association (PCMCIA) bus, or any other bus structure known in the art. First I/O bus 220 couples processor 201 and memory 213 to various other components within A/V device 108, such as for example, mass storage device 221, keyboard controller 222, video controller 226, and audio controller 228.

Mass storage device 221 represents a data storage medium such as a hard disk drive, a floppy disk drive, a CD-ROM device, a flash memory device or any other such mass storage device known in the art to store data. In one embodiment, mass storage device stores instructions and/or code that when executed by processor 201, causes A/V device 108 to perform all or some of the functions described herein. Keyboard controller 222 represents a user input interface for use with a keyboard or pointing device such as a mouse. Video controller 226 represents an interface that enables coupling of a display device (not shown) to A/V device 108. Video controller 226 may represent any of the various graphics adapter cards known in the art to display data on a display device, while audio controller 228 represents an interface that operates to coordinate the recording and rendering of audio in A/V device 108.

Bridge 225 is coupled to both I/O bus 220 and second I/O bus 250 and functions to pass data signals between the two buses. Like first I/O bus 220, second I/O bus 250 may also represent one or more data buses such as an IEEE 1394 backplane, a Peripheral Component Interconnect (PCI) bus, a Personal Computer Memory Card International Association (PCMCIA) bus, or any other bus structure known in the art. It should be noted, however, that the existence of multiple buses is not required in order to practice the present invention. For example, either one or both of network controller 252 and synchronizer 254 may be coupled to first I/O bus 220 rather than second I/O bus 250 as shown in Figure 2. Likewise, any or all of the components coupled to first I/O bus 220 may be coupled to second I/O bus 250 without departing from the spirit and scope of the invention.

Network controller 252 communicatively links A/V device 108 to any number of external data networks such as for example, isochronous network 104. In one embodiment, network controller 252 includes logic to implement an IEEE 1394 compliant physical layer (PHY) providing isochronous signaling to isochronous network 104 through isochronous signal line 257. In another embodiment network controller 252 provides internal isochronous signaling to A/V device 108 via second I/O bus 250 to implement an IEEE 1394 backplane. Upon receiving an isochronous network packet, network controller 252 separates packet header information from packet data. In one embodiment, the packet data is passed to various components of A/V device 108 including processor 201 by way of second I/O bus 250. In one embodiment, network controller 252 also functions to recover timestamp information from the received isochronous packet headers. As each timestamp is recovered, it is forwarded to synchronizer 254 through, for example, side-band connection 253. In other embodiments, the timestamp information may equivalently be passed to synchronizer 254 through second I/O bus 250.

Synchronizer 254 represents logic equipped to synchronize the operating frequency of A/V device 108 with that of other devices, such as A/V device 110. In one embodiment, synchronizer 254 utilizes a house reference signal 255 distributed via reference signal line 102 for example, to synchronize such operating frequencies. Further, synchronizer 254 enables data based in one time domain (i.e. house reference time domain) to be transmitted over an isochronous network in terms of a second time domain (i.e. that defined by an isochronous cycle master). For example, processor 201 replays stored video frames at a designated rate (typically measured in frames per second - fps) proportional to the operating frequency at which the frames were

originally generated and/or recorded. In contrast, isochronous networks, such as isochronous transport medium 104, transmit data based upon time constraints determined by a cycle master. In the event that an A/V device is coupled to both an isochronous network and a house reference signal that operates asynchronously to the cycle time of the isochronous network, time-sensitive data streams generated with respect to the house reference signal may be adversely affected by transmission across the isochronous network.

Figure 3 is a block diagram illustrating one embodiment of synchronizer 254 depicted in Figure 2. Referring to Figure 3, synchronizer 254 includes local clock 302, frame rate converter 304, locking logic 306 and counters 305 and 307. Local clock 302 represents an oscillator known in the art to produce a series of clock pulses. Local clock 302 may provide timing signals for all or some of the components of A/V device 108 shown in Figure 2. Similarly, various clock sources in addition to local clock 302 may also be utilized within A/V device 108.

Although local clock 302 may produce a consistent clock pulse within A/V device 108, typically there is no guarantee other A/V devices within a common system, such as A/V device 110 of Figure 1, will operate at the same frequency. Even if the devices are designed to operate at the same nominal frequency, slight variations between the respective operating frequencies may nonetheless result. Additionally, the clock sources may drift from one another if the operating frequencies are not locked to common signal. Therefore, to avoid the occurrence of such "clock drift," a consistent house reference signal is typically routed to each of the A/V devices. Accordingly, each of the A/V devices may lock their respective operating frequencies to the substantially

fixed frequency of the house reference signal. In one embodiment of the present invention, local clock 302 includes logic to lock the operating frequency of local clock 302 to house reference signal 255.

Frame rate converter 304 represents logic known in the art to produce a desired synchronous output signal based upon a substantially fixed input frequency such as that provided by clock output 309. In one embodiment, frame rate converter 304 generates video clock signal 310 measured in frames per second, based on clock output 309. In addition to handling video data, frame rate converter 304 is similarly equipped to sample audio data. Frame rate converter 304 may sample audio data for example, at a nominal rate of 48,000 samples per second based on clock output 309.

Synchronizer 254 also includes isochronous signal line 357. Isochronous signal line 357 supplies isochronous network packets including timing information to synchronizer 254. In one embodiment, isochronous signal line 357 represents side-band connection 253, whereas in other embodiments, isochronous signal line 357 represents second I/O bus 250. Counters 305 and 307 sample the respective operating frequencies of clock output 309 and isochronous signal line 357 before being fed into locking logic 306.

Locking logic 306 represents logic to lock a first input signal operating at a first frequency to a second input signal operating at a second frequency. In one embodiment, locking logic 306 locks clock output 309 to the operating frequency of isochronous signal line 357 resulting in a locked cycle time 312. Locking logic 306 also includes logic to determine offset and scale factors between the two input signals. In

one embodiment, a scale factor represents the magnitude by which the frequencies of the input signals vary, whereas an offset factor represents the amount in time that one frequency leads or lags the other frequency. In one embodiment the locked cycle time 312 is ignored, whereas the offset and scale factors are further utilized to modify video clock signal 310.

Figure 4 is a block diagram illustrating one embodiment of locking logic 306. Locking logic 306 includes filter block 402, scale block 404, offset block 406, and feedback loop 401. In one embodiment, locking logic 306 utilizes a modified phase lock loop design to determine the offset and scale factors described herein. In one embodiment, locking logic 306 differences an isochronous time signal with a locked cycle time signal supplied by feedback loop 401. In one embodiment, the isochronous time signal is an IEEE 1394 isochronous time signal received on isochronous signal line 357. The difference between the isochronous time signal and the locked cycle time signal is fed through a low pass filter represented by filter block 402. From the filtered signal, both scale and offset factors are determined by scale block 404 and offset block 406 respectively. The scale factor is applied to a local clock signal such as, for example, clock output 309. The offset factor is then applied to the scaled local clock signal, resulting in locked cycle time 312. In one embodiment, the resulting locked cycle time 312 is not further utilized other than for feedback purposes.

By modifying video clock signal 310 an amount equivalent to the determined scale and offset factors, it is therefore possible to represent video clock signal 310 in terms of isochronous time. Stated another way, data recorded and/or generated based on a reference time domain (i.e. local clock 302 alone or in combination with house

reference signal 255) may be represented in terms of the transport time domain (i.e. that of isochronous transport medium 104). For example, using such a conversion scheme, it is possible to predict what the isochronous time should be for a particular video frame that is to be transmitted at some time in the future. Additionally, just as video clock signal 310 may be represented in terms of isochronous time, data received on isochronous signal line 357 may likewise be represented in terms of video clock time.

Thus, a method and apparatus for generating timestamps for isochronous data has been disclosed. In the foregoing specification, the invention has been described with reference to specific embodiments thereof. It will, however, be evident that various modifications and changes can be made thereto without departing from the broader spirit and scope of the invention. The specification and drawings are, accordingly, to be regarded in an illustrative rather than a restrictive sense.

CLAIMS

What is claimed is:

1. A method comprising:

receiving a first signal defining a reference time domain;

receiving a second signal defining a transport time domain asynchronous to the reference time domain; and

generating an isochronous network packet including a timestamp indicating a point in time measured with respect to the reference time domain and represented as a measure of the transport time domain.

2. The method of claim 1, further comprising:

determining an output signal based at least in part upon the first signal;

dynamically sampling the first signal and the second signal to determine a scale factor and an offset factor between the reference and transport time domains; and

modifying the output signal by at least one of the scale factor and the offset factor to represent the output signal in terms of the transport time domain.

3. The method of claim 2, wherein receiving the first signal comprises receiving a house reference signal.

4. The method of claim 1, wherein receiving the second signal comprises receiving at least one isochronous network packet including a timestamp indicating an isochronous network cycle-time.

5. The method of claim 4, wherein the isochronous network cycle time is determined by an IEEE 1394 cycle master device.

6. The method of claim 1, wherein generating the isochronous network packet includes associating the timestamp with at least one frame of generated video data to be transmitted across an isochronous network.

7. The method of claim 1, wherein generating the isochronous network packet includes associating the timestamp with at least one frame of received video data to be transmitted across an isochronous network.

8. An article of manufacture comprising a machine readable medium having a plurality of machine readable instructions stored thereon, wherein when executed by a processor, the instructions cause the processor to:

receive a first signal defining a reference time domain;

receive a second signal defining a transport time domain asynchronous to the reference time domain; and

generate an isochronous network packet including a timestamp indicating a point in time measured with respect to the reference time domain and represented as a measure of the transport time domain.

9. The article of manufacture of claim 8, comprising machine readable instructions that when executed, further cause the processor to:

determine an output signal based at least in part upon the first signal;

dynamically sample the first signal and the second signal to determine a scale factor and an offset factor between the reference and transport time domains; and

modify the output signal by at least one of the scale factor and the offset factor to represent the output signal in terms of the transport time domain.

10. The article of manufacture of claim 9, wherein the machine readable instructions that cause the processor to receive the first signal further cause the processor to receive a house reference signal.

11. The article of manufacture of claim 8, wherein the machine readable instructions that cause the processor to receive the second signal further cause the processor to receive at least one isochronous network packet including a timestamp indicating an isochronous network cycle-time.

12. The article of manufacture of claim 11, wherein the isochronous network cycle time is determined by an IEEE 1394 cycle master device.

13. The article of manufacture of claim 8, wherein the machine readable instructions that cause the processor to generate the isochronous network packet further cause the processor to associate the timestamp with at least one frame of generated video data to be transmitted across an isochronous network.

14. The article of manufacture of claim 8, wherein the machine readable instructions that cause the processor to generate the isochronous network packet further cause the

processor to associate the timestamp with at least one frame of received video data to be transmitted across an isochronous network.

15. An apparatus comprising:

means for receiving a first signal defining a reference time domain;

means for receiving a second signal defining a transport time domain asynchronous to the reference time domain; and

means for generating an isochronous network packet including a timestamp indicating a point in time measured with respect to the reference time domain and represented as a measure of the transport time domain.

16. The apparatus of claim 15, further comprising:

means for determining an output signal based at least in part upon the first signal;

means for dynamically sampling the first signal and the second signal to determine a scale factor and an offset factor between the reference and transport time domains; and

means for modifying the output signal by at least one of the scale factor and the offset factor to represent the output signal in terms of the transport time domain.

17. The apparatus of claim 16, wherein the means for receiving the first signal comprises means for receiving a house reference signal.

18. The apparatus of claim 15, wherein means for receiving the second signal comprises means for receiving at least one isochronous network packet including a timestamp indicating an isochronous network cycle-time.

19. The apparatus of claim 15, wherein the means for generating the isochronous network packet includes means for associating the generated timestamp with at least one frame of generated video data to be transmitted across an isochronous network.

20. The apparatus of claim 15, wherein the means for generating the isochronous network packet includes means for associating the generated timestamp with at least one frame of received video data to be transmitted across an isochronous network.

21. A system comprising:

a communications port to receive a first signal defining a reference time domain; and

a network interface to receive a second signal defining a transport time domain asynchronous to the reference time domain, and to generate an isochronous network packet including a timestamp indicating a point in time measured with respect to the reference time domain and represented as a measure of the transport time domain.

22. The system of claim 21, further comprising:

synchronization logic to:

determine an output signal based at least in part upon the first signal,

dynamically sample the first signal and the second signal to determine a scale factor and an offset factor between the reference and transport time domains, and

modify the output signal by at least one of the scale factor and the offset factor to represent the output signal in terms of the transport time domain.

23. The system of claim 21, wherein the network interface comprises logic to receive at least one isochronous network packet including a timestamp indicating an isochronous network time.

24. The system of claim 22, wherein the synchronization logic further comprises logic to associate the generated timestamp with at least one frame of generated video data to be transmitted across an isochronous network.

25. The system of claim 22, wherein the synchronization logic further comprises logic to associate the generated timestamp with at least one frame of received video data to be transmitted across an isochronous network.

ABSTRACT

A method of generating timestamps for isochronous data includes locking a data stream time and an isochronous network time to a local clock signal such that a bi-directional mapping may be made between the two time domains. Timing information is extracted from both IEEE 1394 based data packets and a conventional house reference signal in order to obtain scale and offset factors that exist between the two signals. The scale and offset factors are applied to a generated video clock signal in order to predict a future video time in terms of IEEE 1394 time.

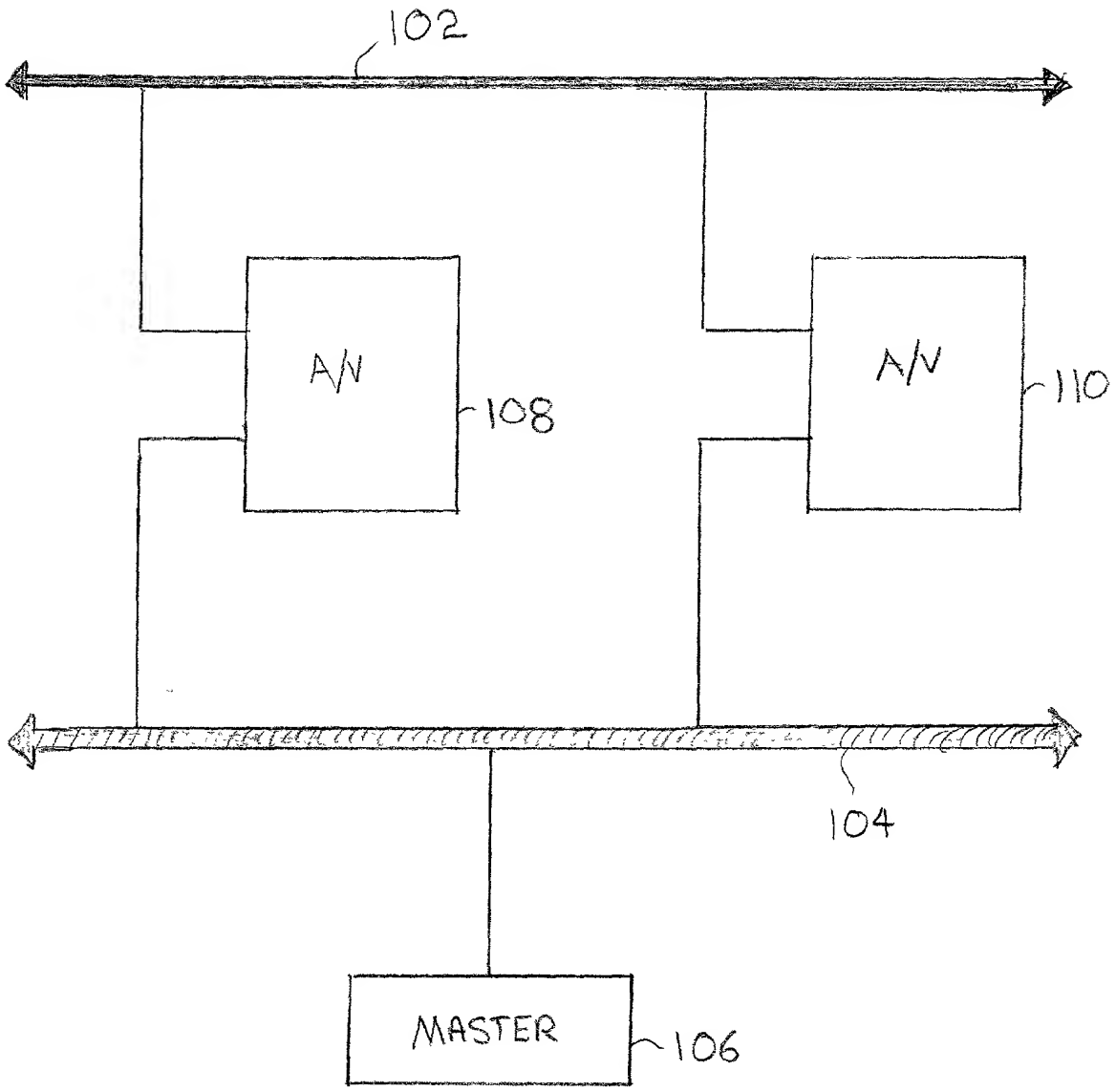
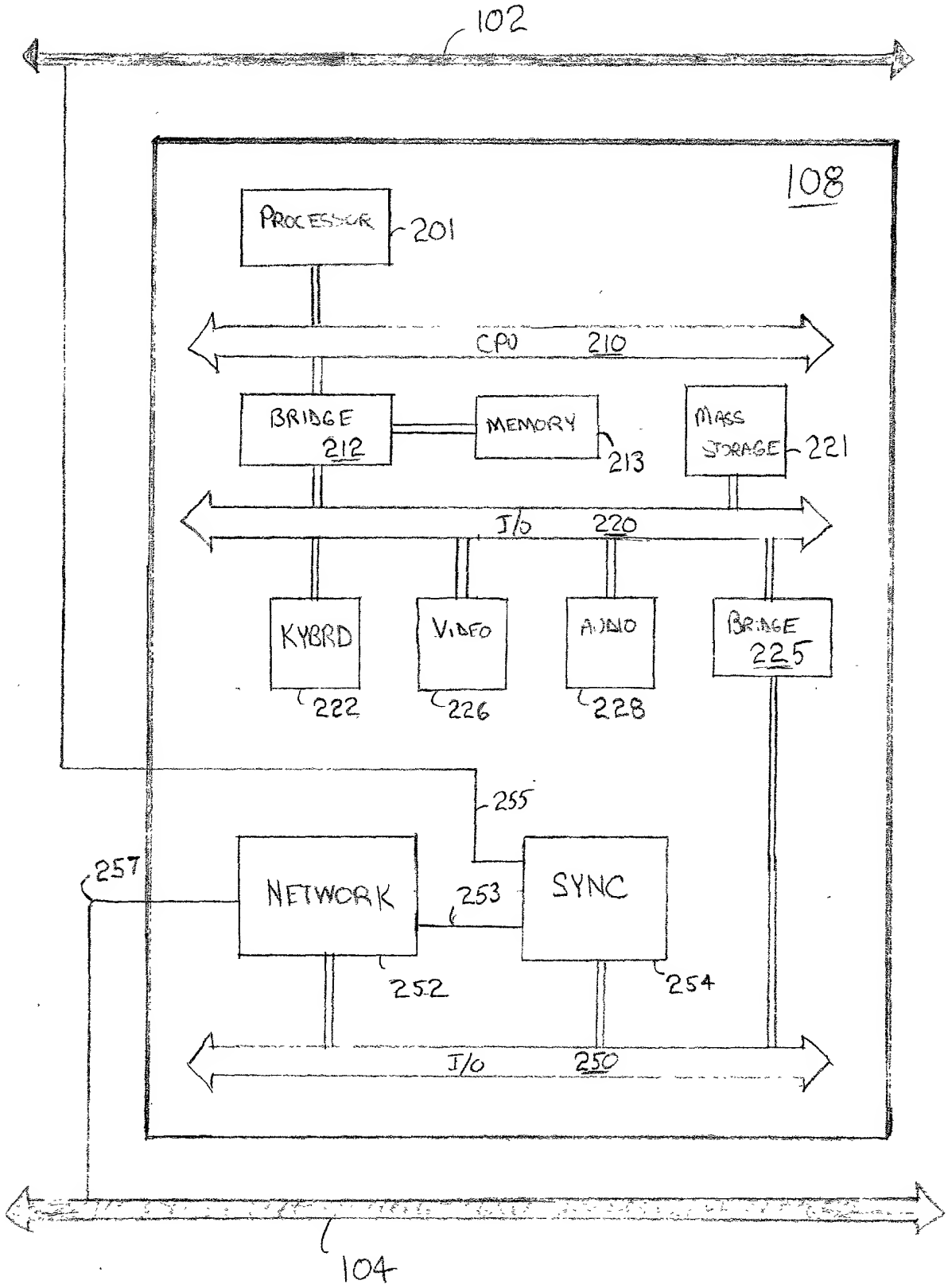


FIG. 1


102
108
PROCESSOR
201
CPU
210
BRIDGE
212
MEMORY
213
MASS STORAGE
221
I/O
220
KYBRD
222
VIDEO
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254
I/O
250
104

FIG. 2

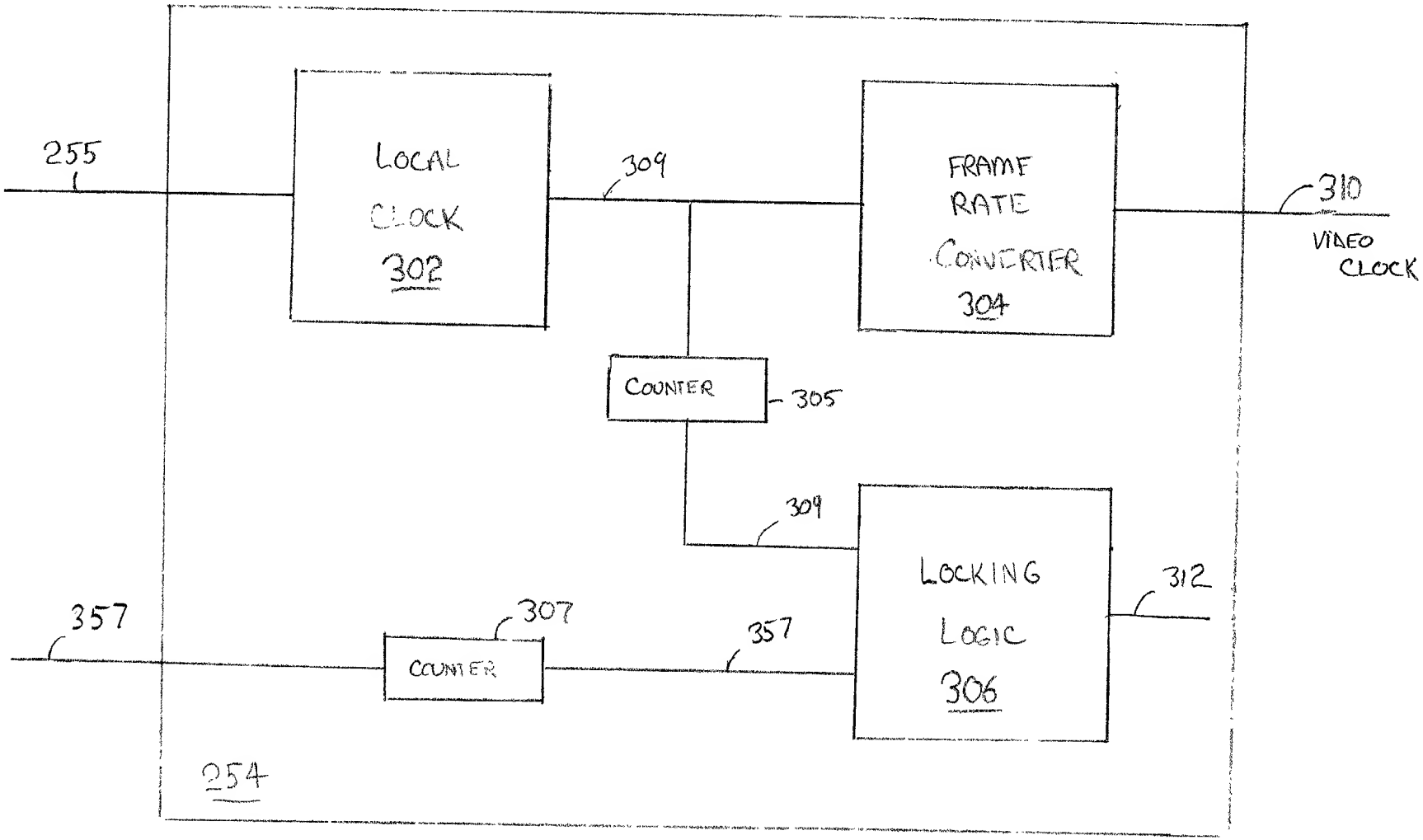

FIG. 3

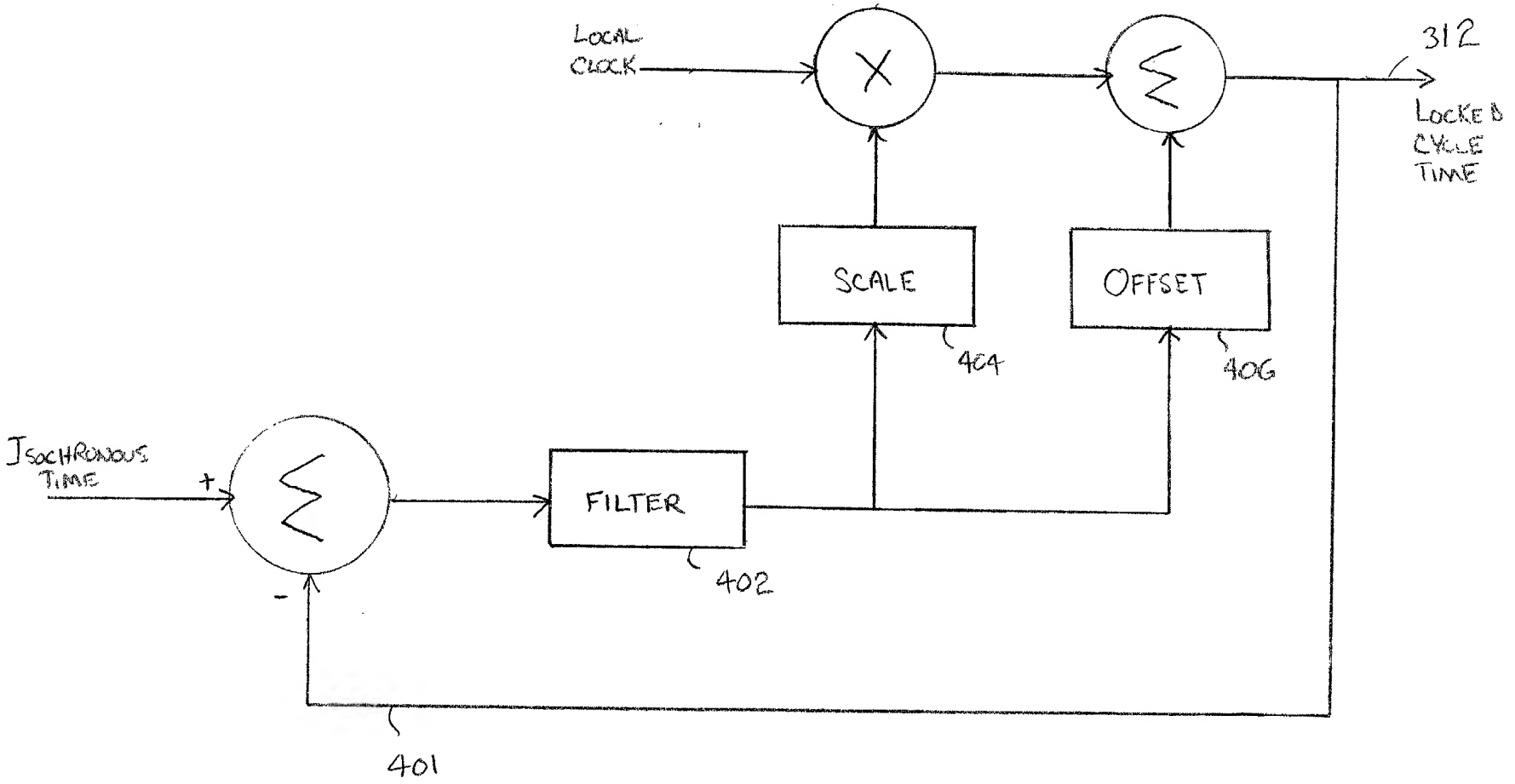

FIG. 4

Attorney's Docket No.: 004509.P005

DECLARATION AND POWER OF ATTORNEY FOR PATENT APPLICATION

As a below named inventor, I hereby declare that:

My residence, post office address and citizenship are as stated below, next to my name.

I believe I am the original, first, and sole inventor (if only one name is listed below) or any original, first, and joint inventor (if plural names are listed below) of the subject matter which is claimed and for which a patent is sought on the invention entitled

A METHOD OF GENERATING TIMESTAMPS FOR ISOCHRONOUS DATA

the specification of which
- [X] is attached hereto.
- [ ] was filed on _____ as
  United States Application Number _____
  or PCT International Application Number _____
  and was amended on _____

(if applicable)

I hereby state that I have reviewed and understand the contents of the above-identified specification, including the claim(s), as amended by any amendment referred to above. I do not know and do not believe that the claimed invention was ever known or used in the United States of America before my invention thereof, or patented or described in any printed publication in any country before my invention thereof or more than one year prior to this application, that the same was not in public use or on sale in the United States of America more than one year prior to this application, and that the invention has not been patented or made the subject of an inventor's certificate issued before the date of this application in any country foreign to the United States of America on an application filed by me or my legal representatives or assigns more than twelve months (for a utility patent application) or six months (for a design patent application) prior to this application.

I acknowledge the duty to disclose all information known to me to be material to patentability as defined in Title 37, Code of Federal Regulations, Section 1.56.

I hereby claim foreign priority benefits under Title 35, United States Code, Section 119(a)-(d), of any foreign application(s) for patent or inventor's certificate listed below and have also identified below any foreign application for patent or inventor's certificate having a filing date before that of the application on which priority is claimed:

Prior Foreign Application(s):

APPLICATION NUMBER	COUNTRY (OR INDICATE IF PCT)	DATE OF FILING (day, **month**, year)	PRIORITY CLAIMED UNDER 37 USC 119
			☐ No ☐ Yes
			☐ No ☐ Yes
			☐ No ☐ Yes

I hereby claim the benefit under Title 35, United States Code, Section 119(e) of any United States provisional application(s) listed below:

APPLICATION NUMBER	FILING DATE

I hereby claim the benefit under Title 35, United States Code, Section 120 of any United States application(s) listed below and, insofar as the subject matter of each of the claims of this application is not disclosed in the prior United States application in the manner provided by the first paragraph of Title 35, United States Code, Section 112, I acknowledge the duty to disclose all information known to me to be material to patentability as defined in Title 37, Code of Federal Regulations, Section 1.56 which became available between the filing date of the prior application and the national or PCT international filing date of this application:

APPLICATION NUMBER	FILING DATE	STATUS (ISSUED, PENDING, ABANDONED)

I hereby appoint the persons listed on Appendix A hereto (which is incorporated by reference and a part of this document) as my respective patent attorneys and patent agents, with full power of substitution and revocation, to prosecute this application and to transact all business in the Patent and Trademark Office connected herewith.

Send correspondence to:
Thomas M. Coester, Reg. No. 39,637, BLAKELY, SOKOLOFF, TAYLOR & ZAFMAN, LLP
(Name of Attorney or Agent)
12400 Wilshire Boulevard, 7th Floor, Los Angeles, California 90025 and direct telephone calls to:
Thomas M. Coester, (503) 684-6200.
(Name of Attorney or Agent)

I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code and that such willful false statements may jeopardize the validity of the application or any patent issued thereon.

Full Name of Sole/First Inventor (given name, family name) **Richard Wissler Stallkamp**

Inventor's Signature Richard Wissler Stallkamp Date 3/30/2000

Residence Tigard, Oregon USA Citizenship USA
(City, State) *(Country)*

P. O. Address 14698 S.W. Rask Terrace
Tigard, Oregon 97224 USA

Full Name of Second/Joint Inventor (given name, family name) _____

Inventor's Signature _____ Date _____

Residence _____ Citizenship _____
(City, State) *(Country)*

P. O. Address _____

Appendix A

I hereby appoint BLAKELY, SOKOLOFF, TAYLOR & ZAFMAN LLP, a firm including: William E. Alford, Reg. No. 37,764; Farzad E. Amini, Reg. No. 42,261; Amy M. Armstrong, Reg. No. 42,265; Aloysius T. C. AuYeung, Reg. No. 35,432; William Thomas Babbitt, Reg. No. 39,591; Carol F. Barry, Reg. No. 41,600; Jordan Michael Becker, Reg. No. 39,602; Bradley J. Bereznak, Reg. No. 33,474; Michael A. Bernadicou, Reg. No. 35,934; Roger W. Blakely, Jr., Reg. No. 25,831; Gregory D. Caldwell, Reg. No. 39,926; Ronald C. Card, Reg. No. 44,587; Thomas M. Coester, Reg. No. 39,637; Donna Jo Coningsby, Reg. No. 41,684; Michael Anthony DeSanctis, Reg. No. 39,957; Daniel M. De Vos, Reg. No. 37,813; Robert Andrew Diehl, Reg. No. 40,992; Matthew C. Fagan, Reg. No. 37,542; Tarek N. Fahmi, Reg. No. 41,402; James Y. Go, Reg. No. 40,621; James A. Henry, Reg. No. 41,064; Willmore F. Holbrow III, Reg. No. 41,845; Sheryl Sue Holloway, Reg. No. 37,850; George W Hoover II, Reg. No. 32,992; Eric S. Hyman, Reg. No. 30,139; Dag H. Johansen, Reg. No. 36,172; William W. Kidd, Reg. No. 31,772; Eric T. King, Reg. No. 44,188; Erica W. Kuo, Reg. No. 42,775; Michael J. Mallie, Reg. No. 36,591; Paul A. Mendonsa, Reg. No. 42,879; Darren J. Milliken, Reg. No. 42,004; Chun M. Ng, Reg. No. 36878; Thien T. Nguyen, Reg. No. 43,835; Thinh V. Nguyen, Reg. No. 42,034; Dennis A. Nicholls, Reg. No. 42,036; Lisa A. Norris, Reg. No. 44,976; Daniel E. Ovanezian, Reg. No. 41,236; Babak Redjaian, Reg. No. 42,096; William F. Ryann, Reg. No. 44,313; James H. Salter, Reg. No. 35,668; William W. Schaal, Reg. No. 39,018; James C. Scheller, Reg. No. 31,195; Jeffrey S. Smith, Reg. No. 39,377; Maria McCormack Sobrino, Reg. No. 31,639; Stanley W. Sokoloff, Reg. No. 25,128; Judith A. Szepesi, Reg. No. 39,393; Vincent P. Tassinari, Reg. No. 42,179; Edwin H. Taylor, Reg. No. 25,129; George G. C. Tseng, Reg. No. 41,355; Joseph A. Twarowski, Reg. No. 42,191; Lester J. Vincent, Reg. No. 31,460; Glenn E. Von Tersch, Reg. No. 41,364; John Patrick Ward, Reg. No. 40,216; Charles T. J. Weigell, Reg. No. 43,398; Kirk D. Williams, Reg. No. 42,229; James M. Wu, Reg. No. P45,241; Steven D. Yates, Reg. No. 42,242; and Norman Zafman, Reg. No. 26,250; my attorneys; and Andrew C. Chen, Reg. No. 43,544; Justin M. Dillon, Reg. No. 42,486; Paramita Ghosh, Reg. No. 42,806; Sang Hui Kim, Reg. No. 40,450; and John F. Travis, Reg. No. 43,203; my patent agents, with offices located at 12400 Wilshire Boulevard, 7th Floor, Los Angeles, California 90025, telephone (714) 557-3800, with full power of substitution and revocation, to prosecute this application and to transact all business in the Patent and Trademark Office connected herewith.